[Document] SPECIFICATION

[Title of the Invention] SEMICONDUCTOR DEVICE

[What is claimed is:]

[Claim 1] A semiconductor device characterized by comprising:

a Cu film which constitutes a wiring layer;

an intermediate layer formed on the Cu film; and

an Al film formed on the intermediate layer and used as a pad;

wherein the intermediate layer comprises a metal nitride film having a high melting point and a metal film having a high melting point formed on the metal nitride film having a high melting point.

[Claim 2] A semiconductor device characterized by comprising:

a Cu film which constitutes a wiring layer;

an intermediate layer formed on the Cu film; and

an Al film formed on the intermediate layer and used as a pad;

wherein the intermediate layer comprises a metal film having a high melting point and a metal nitride film having a high melting point formed on the metal film having a high melting point.

[Claim 3] The semiconductor device according to claim 1 or claim 2, characterized in that

a metal element contained in the metal film having a high melting point is the same as a metal element

contained in the metal nitride film having a high melting point.

[Claim 4] The semiconductor device according to claim 1 or claim 2, characterized in that

a metal element contained in the metal film having a high melting point and a metal element contained in the metal nitride film having a high melting point are respectively selected from among Ta, Nb, Ti and V.

[Claim 5] A semiconductor device characterized by comprising:

a Cu film which constitutes a wiring layer;

an intermediate layer formed on the Cu film; and

an Al film formed on the intermediate layer and used as a pad;

wherein the intermediate layer comprises a first metal film having a high melting point, a metal nitride film having a high melting point formed on the first metal film having a high melting point, and a second metal film having a high melting point formed on the metal nitride film having a high melting point.

[Claim 6] The semiconductor device according to claim 5, characterized in that

a metal element contained in the first metal film having a high melting point, a metal element contained in the metal nitride film having a high melting point and a metal element contained in the second metal film having a high melting point are the same.

[Claim 7] The semiconductor device according to claim 5, characterized in that

a metal element contained in the first metal film having a high melting point, a metal element contained in the metal nitride film having a high melting point, and a metal element contained in the second metal film having a high melting point are respectively selected from among Ta, Nb, Ti, and V.

[Detailed Description of the Invention]

[0001]

[Technical Field of the Invention]

The present invention relates to a semiconductor device represented by an LSI, and more particularly to a connection between a Cu film for wiring and an Al film for a pad.

[0002]

[Prior Art]

FIG. 10 is a sectional view showing a structure of a conventional semiconductor device having the Cu film for wiring and the Al film for the pad.

[0003]

In an example shown in FIG. 10 there is shown a state in which a second layer region (comprising an interlayer insulating film 21, a barrier layer 22 and a Cu film 23 for wiring) is formed on a first layer region (an interlayer insulating film 11, a barrier layer 12 and a metal film 13 for wiring), and a third layer region (a silicon nitride film 31, an upper layer insulating film 32, a barrier layer

33 and an Al film 34 for a pad) are formed on the second layer region.

[0004]

As shown in FIG. 10, a barrier layer 33 is provided between the Cu film 23 for wiring and the Al film 34 for the pad. This barrier layer 33 is provided for preventing a mutual diffusion between the Cu film 23 and the Al film 34. For a barrier metal, a metal nitride having a high melting point such as TaN, NbN, TiN, VN or the like is used.

[0005]

However, in the prior art, there is a problem in that when the Al film 34 is formed by the sputtering method or the like, Al contained in the Al film 34 and the N contained in the barrier layer 33 are allowed to react with each other to form AlN_X which is an insulator so that the resistance (particularly via resistance) is raised with AlN_X. Furthermore, there is also a problem in that since adherence between the silicon oxide film used for the upper layer insulating film 32 and the metal nitride film having a high melting point used for the barrier layer 33 is poor, oxide invades from a gap between the silicon oxide film and the metal nitride film having a high melting point with the result that the Cu film 23 is oxidized.

[0006]

[Objects of the Invention]

In this manner, in order to prevent mutual diffusion between the Cu film for wiring and the Al film for the pad,

a metal nitride film having a high melting point is provided as a barrier layer between the Cu film and the Al film. However, there is a problem in that a resistance is raised because of AlN_X formed with a reaction between Al and N. There is also a problem in that the Cu film is oxidized because of poor adherence between the upper layer insulating film and the barrier layer. Thus, this leads to the deterioration of characteristic and reliability of the semiconductor device.

[0007]

The present invention has been made in view of the conventional problem. An object of the present invention is to provide a semiconductor device having a Cu film for wiring and an Al film for a pad connected to the Cu film, wherein a characteristic and reliability thereof can be improved.

[0008]

[Means for Achieving the Objects]

According to a first aspect of the present invention, there is provided a semiconductor device characterized by comprising a Cu film which constitutes a wiring layer; an intermediate layer formed on the Cu film; and an Al film formed on the intermediate layer and used as a pad; wherein the intermediate layer comprises a metal nitride film having a high melting point and a metal film having a high melting point formed on the metal nitride film having a high melting point.

[0009]

According to the present invention, there is obtained a structure in which a metal film having a high melting point is sandwiched between the Al film and the metal nitride film having a high melting point. Consequently, the fact that Al contained in the Al film and N contained in the metal nitride film having a high melting point are allowed to react with each other to form AlN_X which is an insulator can be prevented. Thus, the problem in that the resistance is raised with AlN_X can be prevented so that a semiconductor device with an excellent characteristic can be obtained.

[0010]

According to a second aspect of the present invention, there is provided a semiconductor device characterized by comprising a Cu film which constitutes a wiring layer; an intermediate layer formed on the Cu film; and an Al film formed on the intermediate layer and used as a pad; wherein the intermediate layer comprises a metal film having a high melting point and a metal nitride film having a high melting point formed on the metal film having a high melting point.

[0011]

According to the present invention, since the metal film having a high melting point having more excellent adherence to the insulating film such as a silicon oxide based insulating film or the like than the metal nitride film having a high melting point is formed under the metal nitride film having a high melting point, adherence between

the intermediate layer and the insulating film contacting the intermediate layer is improved. Consequently, it is possible to prevent the problem in that oxygen invades from a gap generated by adherence failure so that the Cu film is oxidized. Thus, it becomes possible to manufacture a semiconductor device having excellent reliability.

[0012]

According to the first and the second aspects of the invention, it is preferable that a metal element contained in the metal film having a high melting point is the same as a metal element contained in the metal nitride film having a high melting point. By using the same metal element having a high melting point in this manner, the same sputtering target can be used at the time of forming the metal film having a high melting point and forming the metal nitride film having a high melting point. Thus, the manufacturing step can be shortened and the manufacturing cost can be decreased.

[0013]

According to the first and the second aspects of the present invention, it is preferable that a metal element contained in the metal film having a high melting point and a metal element contained in the metal nitride film having a high melting point are respectively selected from among Ta (tantalum), Nb (niobium), Ti (titanium), and V (vanadium).

[0014]

According to a third aspect of the present invention,

there is provided a semiconductor device characterized by comprising a Cu film which constitutes a wiring layer; an intermediate layer formed on the Cu film; and an Al film formed on the intermediate layer and used as a pad; wherein the intermediate layer comprises a first metal film having a high melting point, a metal nitride film having a high melting point formed on the first metal film having a high melting point, and a second metal film having a high melting point formed on the metal nitride film having a high melting point.

[0015]

According to the present invention, it becomes possible to manufacture a semiconductor device which combines advantages obtained from the first and second aspect of the present invention and has an excellent characteristic and reliability.

[0016]

According to the third aspect of the present invention, it is preferable that a metal element contained in the first metal film having a high melting point, a metal element contained in the metal nitride film having a high melting point and a metal element contained in the second metal film having a high melting point are the same. By using the same metal element having a high melting point in this manner, the same sputtering target can be used at the time of forming the first and second metal film having a high melting point and the metal nitride film having a high

melting point. Thus, the manufacturing step can be shortened and the manufacturing cost can be decreased.

[0017]

According to the third aspect of the present invention, it is preferable that a metal element contained in the first metal film having a high melting point, a metal element contained in the metal nitride film having a high melting point, and a metal element contained in the second metal film having a high melting point are respectively selected from among Ta, Nb, Ti, and V.

[0018]

[Embodiments of the Invention]

Hereinafter, referring to the drawings, embodiments of the present invention will be explained.

[0019]

(First Embodiment)

FIGS. 1 (a) through 2 (g) are sectional views showing a method for manufacturing the semiconductor device according to a first embodiment of the present invention.

[0020]

In the beginning, as shown in FIG. 1 (a), on the main surface side of the semiconductor substrate (not shown) on which the semiconductor device (not shown) such as a transistor or the like is formed, an interlayer insulating film 11, barrier layer 12 and metal film 13 for wiring are formed as the first layer region. Furthermore, an interlayer insulating film 21 (for example, TEOS-SiO_2

film or the Low-k (low dielectric constant) film, or a lamination layer thereof) of the second layer region is formed thereon. While the first layer region is shown as a bottom layer as a matter of convenience, lower layer regions may be provided under the first layer region.

[0021]

Next, as shown in FIG. 1 (b), the interlayer insulating film 21 is processed to form a via hole, and a groove for the wiring and the pad.

[0022]

Next, as shown in FIG. 1 (c), as the barrier layer (barrier metal layer) 22, a metal nitride film having a high melting point (such as TaN, NbN or the like) is formed on an overall surface. Furthermore, a Cu film 23 is formed on the barrier layer 22. The Cu film 23 is obtained by forming on the barrier layer 22 a Cu film which constitutes a seed layer and forming the Cu film by means of the electrolytic plating process.

[0023]

Next, as shown in FIG. 1 (d), a planarization processing is carried out with the CMP process so that a barrier layer 22 and the Cu film 23 are retained only inside the via hole, and the groove for the wiring and the pad. In this processing, the via, the wiring and the pad of the second layer region are formed.

[0024]

After that, when the insulating film such as the

TEOS-SiO_2 film or the Low-k (a low dielectric constant) film or the like is formed as a passivation film, and the hole for the pad is formed for assembly in the insulating film, so that the surface of the Cu pad portion is exposed. As a consequence, the Cu pad portion is oxidized, and oxidation progresses with the lapse of time so that the Cu wiring as a whole is oxidized. Then, in order to prevent the oxidation of the Cu pad, an Al pad region is formed as a third layer region on the top layer. In this embodiment, a dual damascene process is used for the formation of the Al pad region shown in FIGS. 2 (e) through 2 (g).

[0025]

As shown in FIG. 2 (e), in order to prevent the diffusion of Cu contained in the Cu film 23, a silicon nitride film (plasma SiN film) 31 is formed on the overall surface. Subsequently, an upper layer insulating film 32 (for example, TEOS-SiO_2 film or a Low-k (low dielectric constant) film, or a lamination layer film thereof) is formed on the silicon nitride film 31. After that, the silicon nitride film 31 and the upper layer insulating film 32 are processed to form a via hole and a groove for the pad.

[0026]

Next as shown in FIG. 2 (f), an intermediate layer 33 having a structure as described later is formed on the overall surface. Furthermore, an Al film 34 is formed on the intermediate layer 33 with the sputtering process (long throw sputtering or a reflow sputtering is preferable) or

the like.

[0027]

Furthermore, as shown in FIG. 2 (g), the planarization processing is carried out with the CMP process to allow the intermediate layer 33 and the Al film 34 to be retained only in the via hole and the groove for the pad. With this processing, the via and the pad for the third layer region are formed.

[0028]

FIGS. 3 (a) through 3 (c) are views showing some examples of the structure of the above described intermediate layer 33.

[0029]

The structure of FIG. 3 (a) is an example in which a lamination layer structure of a metal nitride film having a high melting point 33b (for example, a barrier metal layer such as TaN film or the like), and a metal film having a high melting point 33c (for example, Ta film or the like) are used as the intermediate layer 33. The conventional problem can be prevented by sandwiching the metal film having a high melting point 33C between the Al film 34 and the metal nitride film having a high melting point 33b. That is, the problem in that Al contained in the Al film 34 and N contained in the metal nitride film having a high melting point 33b are allowed to react with each other to form AlN_X which is an insulator can be prevented. Thus, the problem in that the resistance (particularly,

via resistance) is raised with AlN_X can be prevented.

[0030]

The structure of FIG. 3 (b) is an example in which a lamination layer structure of the metal film having a high melting point 33a (for example, Ta film or the like) and the metal nitride film having a high melting point 33b (for example, TaN film or the like) is used as the intermediate layer 33. With such a structure, the metal film having a high melting point 33a having an excellent adhesiveness is sandwiched between the metal nitride film having a high melting point 33b and the upper layer insulating film 32 formed of silicon oxide film type insulating film, so that the adhesiveness between the intermediate layer 33 and the upper layer insulating film 32 is improved. Consequently, it is possible to prevent the problem in that oxygen invades from a gap generated by adherence failure between the intermediate layer 33 and the upper layer insulating film 32 so that the Cu film 23 is oxidized.

[0031]

The structure of FIG. 3 (c) is an example in which a lamination structure of the metal film having a high melting point 33a (for example, Ta film or the like), the metal nitride film having a high melting point 33b (for example, TaN film or the like) and the metal film having a high melting point 33c (for example, Ta film or the like) is used as the intermediate layer 33, and both effects obtained in the structure of FIG. 3 (a) and FIG. 3 (b) can

be obtained.

[0032]

Incidentally, in the metal films having a high melting point 33a and 33c, any of a Ta film, an Nb film, a Ti film, or a V film can be used. In the metal nitride film having a high melting point 33b, any one of a TaN film, an NbN film, a TiN film, or a VN film can be used.

[0033]

Furthermore, in each structure of FIGS. 3 (a) through 3 (c), the metal element having a high melting point contained in the metal film having a high melting point and the metal element having a high melting point contained in the metal nitride film having a high melting point may be different from each other. However, it is preferable that the metal element having a high melting point contained in the metal film having a high melting point and the metal element having a high melting point contained in the metal nitride film having a high melting point are the same. In the structure of FIG. 3 (c), it is preferable that the metal elements having a high melting point contained in the metal film having a high melting point 33a, the metal nitride film having a high melting point 33b and the metal film having a high melting point 33c are the same. Since the same sputtering target can be used at the time of forming each film by sputtering through use of the same metal element having a high melting point in this manner, an attempt can be made to shorten the manufacturing step and decrease the

cost thereof.

[0034]

Furthermore, the thickness of the metal nitride film having a high melting point is preferably thick from the viewpoint of the barrier while the thickness may be preferably thin from the viewpoint of the resistance (in particular, the via resistance) and the CMP. FIG. 4 is a view showing a relationship between the thickness of the TaN film and the sheet resistance by changing the annealing condition. As can be seen from FIG. 4, under the EM examination condition of the Cu wiring (450℃ 4 min (reflow sputtering corresponding time) + 400℃ 30 min (sinter corresponding time) + 350℃ 6h (EM examination corresponding time)), it is preferable that the thickness of the TaN film is 20 nm or more. In consideration of heat stress (corresponding to an increase of EM examination time), it is preferable that the thickness of the TaN film is 40 nm or more. Furthermore, it is preferable that the thickness of Ta film is 5 nm or less because the CMP becomes difficult when the thickness is too thick.

[0035]

Furthermore, when a part of the via hole pattern formed in the upper layer insulating film 32 of the third layer region is located outside of the groove pattern for the pad formed in the second layer region, the following disadvantage as shown in FIG. 5 is generated. That is, when the upper layer insulating film 32 and the silicon nitride

film 31 at step of FIG. 2 (e) are over-etched, the interlayer insulating film 21 in the second layer region is also etched, so that a recess shown in FIG. 5 is generated. As a consequence, when the intermediate layer 33 and the Al film 34 are deposited at step of FIG. 2 (f), there is a problem that these films cannot be completely buried in the recess. Consequently, preferably the overall via hole pattern in the third layer region is located at the inside of the groove pattern for the pad in the second layer region.

[0036]

Furthermore, it is preferable that the Al pad portion has a divided pad structure. By using the divided pad structure, decrease in the adhesiveness resulting from a difference in the expansion coefficient between the barrier metal or the like and the silicon oxide film type insulating film can be alleviated.

[0037]

FIG. 6 is a view showing a structure for improving the endurance at the time of wire bonding. That is, a pad portion comprising the Al film 34 and the intermediate layer 33 is extended, so that a bonding wire 40 is connected to the extended region. With such a structure, even when the intermediate layer 33 is penetrated and torn by a bonding wire at the wire bonding, the influence upon the connection portion between the Cu film 23 and the Al film 34 can be suppressed.

[0038]

(Second embodiment)

FIGS. 7 (a) through 7 (c) are sectional views showing a method for manufacturing a semiconductor device according to the second embodiment of the present invention. The second embodiment is an example in which a single damascene process is used in the formation of the Al pad portion of the third layer region. Up to the midst step (FIG. 1 (d)), the second embodiment is the same as the first embodiment, so that the step after that will be explained.

[0039]

After the step shown in FIG. 1 (d), as shown in FIG. 7 (a), in the same manner as the first embodiment, the silicon nitride film (plasma SiN film) 31 is formed on an overall surface. Then, the upper layer insulating film 32 (for example, TEOS-SiO_2 film or Low-k (low dielectric constant) film, or a lamination structure thereof) is formed on the silicon nitride film 31. Thereafter, the silicon nitride film 31 and the upper layer insulating film 32 are processed to form a groove for the pad.

[0040]

Next, as shown in FIG. 7 (b), the intermediate layer 33 is formed on an overall surface. Furthermore, the Al film 34 is formed on the intermediate layer 33 with the sputtering process (long throw sputtering or the reflow sputtering is preferable) or the like. With respect to the intermediate layer 33, the second embodiment is the same as

the first embodiment. That is, the structure of the intermediate layer 33 is a lamination layer structure (a lamination structure of the metal film having a high melting point/metal nitride film having a high melting point, a lamination structure of the metal nitride film having a high melting point/metal film having a high melting point, or a lamination structure of the metal film having a high melting point/metal nitride film having a high melting point/metal film having a high melting point) shown in FIG. 3 (a) through 3 (c). Furthermore, with respect to the material used in the metal film having a high melting point and the metal nitride film having a high melting point and a combination thereof, the second embodiment is the same as the first embodiment.

[0041]

Next, as shown in FIG. 7 (c), a pad of the third region is formed by carrying out the planarization processing with the CMP process to allow the intermediate layer 33 and the Al film 34 to be retained in the groove for the pad.

[0042]

FIG. 7 (d) is a sectional view showing an essential portion of a structure corresponding to FIG. 7 (c). When a part of the groove pattern for the pad formed in the upper layer insulating film 32 of the third layer region is located outside of the groove pattern for the pad formed in the second layer region, the same disadvantage as that described in the first embodiment is generated.

Consequently, as described in FIG. 7 (d), preferably the whole groove pattern for the pad in the third layer region is located inside of the groove pattern for the pad in the second layer region.

[0043]

(Third embodiment)

FIGS. 8 (a) through 8 (c) are sectional views showing a method for manufacturing a semiconductor device according to a third embodiment of the present invention. The third embodiment is an example in which the via process and the RIE process are used in the formation of the Al pad portion of the third layer region. Since the third embodiment is the same as the first embodiment up to the midst step (FIG. 1 (d)), the step after that will be explained.

[0044]

After the step shown in FIG. 1 (d), as shown in FIG. 8 (a), the silicon nitride film (plasma SiN film) 31 is formed on an overall surface in the similar manner as described in the first embodiment. Then, the upper layer insulating film 32 (for example, TEOS-SiO_2 film or the Low-k (low dielectric constant) film, or the lamination layer structure thereof) is formed on the silicon nitride film 31. Thereafter, the silicon nitride film 31 and the upper layer insulating film 32 are processed to form a via hole.

[0045]

Next, as shown in FIG. 8 (b), the intermediate layer 33 is formed on an overall surface. Furthermore, an Al film 34

is formed on the intermediate layer 33 with the sputtering process (either long throw sputtering or reflow sputtering is preferable) or the like. With respect to the intermediate layer 33, the third embodiment is the same as the first embodiment. That is, the structure of the intermediate layer 33 is a lamination structure (a lamination structure of the metal film having a high melting point/metal nitride film having a high melting point, a lamination structure of the metal nitride film having a high melting point/metal film having a high melting point, or a lamination structure of the metal film having a high melting point/metal nitride film having a high melting point/metal film having a high melting point) shown in FIGS. 3 (a) through 3 (c). Furthermore, with respect to the material used in the metal film having a high melting point and the metal nitride film having a high melting point, and a combination thereof, the third embodiment is the same as the first embodiment.

[0046]

Next, as shown in FIG. 7 (c), a resist mask (not shown) is used to etch the Al film 34 and the intermediate layer 33 to form a pad of a third region.

[0047]

FIG. 8 (d) is a sectional view showing an essential portion of a structure corresponding to FIG. 8 (c). When a part of the via hole pattern formed in the upper layer insulating film 32 of the third layer region is located

outside of the groove pattern for the pad formed in the second layer region, the same disadvantage as that described in the first embodiment is generated. Consequently, as described in FIG. 8 (d), preferably the whole via hole pattern in the third layer region is located inside of the groove pattern for the pad in the second layer region.

[0048]

(Fourth embodiment)

FIGS. 9 (a) through 9 (c) are sectional views showing a method for manufacturing a semiconductor device according to the fourth embodiment of the present invention. The fourth embodiment is an example in which RIE process is used in the formation of the Al pad of the third layer region. Up to the midst step (FIG. 1(d)), the fourth embodiment is the same as the first embodiment, so that the step after that will be explained.

[0049]

After the step shown in FIG. 1 (d), as shown in FIG. 9 (a), the intermediate layer 33 is formed on an overall surface. Furthermore, the Al film 34 is formed on the intermediate layer 33 with the sputtering process (long throw sputtering is preferable) or the like. With respect to the intermediate layer 33, the fourth embodiment is the same as the first embodiment. That is, the structure of the intermediate layer 33 is a lamination layer structure (a lamination layer structure of the metal film having a high melting point/metal nitride film having a high

melting point, a lamination layer structure of the metal nitride film having a high melting point/metal film having a high melting point, or a lamination structure of the metal film having a high melting point/metal nitride film having a high melting point/metal film having a high melting point) shown in FIG. 3 (a) through 3 (c). Furthermore, with respect to the material used in the metal film having a high melting point and the metal nitride film having a high melting point, and a combination thereof, the fourth embodiment is the same as the first embodiment.

[0050]

Next, as shown in FIG. 9 (b), a pad of the third region is formed by etching the Al film 34 and the intermediate layer 33 by using a resist mask (not shown).

[0051]

FIG. 9 (c) is a sectional view showing an essential portion of a structure corresponding to FIG. 9 (b). Unless the pattern of the Cu pad formed in the second layer region is covered with the Al pad pattern of the third layer region, there arises a disadvantage in that the Cu pad formed in the second layer region is oxidized. Consequently, as shown in FIG. 9 (c), it is preferable that the pad pattern in the third layer region covers the whole pad pattern in the second layer region, that is, the whole pad pattern in the second layer region is located inside of the pad pattern in the third layer region.

[0052]

Embodiments of the present invention have been described above. However, the present invention is not limited to these embodiments, and various modifications may be made without departing from the spirit or scope of the present invention.

[0053]

[Advantages of the Invention]

According to the present invention, lamination structure of the metal film having a high melting point and the metal nitride film having a high melting point applied to the intermediate layer provided between the Cu film which constitutes a wiring layer and the Al film which acts as a pad layer makes it possible to manufacture a semiconductor device having an excellent characteristic and reliability.

[Brief Description of the Drawings]

[FIG. 1]

Sectional views showing a part of a method for manufacturing a semiconductor device according to the first embodiment of the present invention.

[FIG. 2]

Sectional views showing a part of a method for manufacturing a semiconductor device according to the first embodiment of the present invention.

[FIG. 3]

Sectional views showing a structure of a main portion of the semiconductor device according to the first

embodiment of the present invention.

[FIG. 4]

A view showing a relationship between a thickness of a TaN film and a sheet resistance.

[FIG. 5]

A view showing an unfavorable state in a connection between pads.

[FIG. 6]

A view showing a structure for improving endurance at the time of wire bonding in the embodiments of the present invention.

[FIG. 7]

Sectional views showing a part of a method for manufacturing the semiconductor device according to the second embodiment of the present invention.

[FIG. 8]

Sectional views showing a part of a method for manufacturing the semiconductor device according to a third embodiment of the present invention.

[FIG. 9]

Sectional views showing a part of method for manufacturing the semiconductor device according to a fourth embodiment of the present invention.

[FIG. 10]

A sectional view showing a structure of a semiconductor device according to the prior art.

[Explanation of Reference Symbols]

11, 21 ... Interlayer insulting film,

12, 22 ... Barrier layer,

13 ... Metal film,

23 ... Cu film,

31 ... Silicon nitride film,

32 ... Upper layer insulting film,

33 ... Intermediate layer,

33a, 33c ... Metal film having a high melting point,

33b ... Metal nitride film having a high melting point,

34 ... Al film,

40 ... Bonding wire.